REMARKS

Applicant has carefully studied the outstanding Office Action in the present application. The present response is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

The allowability of claims 60-69, 73-74, 76 and 81 is noted with appreciation.

Applicant expresses his appreciation to Examiner Luan Thai for the courtesy of an interview which was granted to Applicants' representative, Sanford T. Colb (Reg. No. 26,856). The interview was held in the USPTO on February 25, 2004.

In the interview, the claims were discussed vis-à-vis the prior art reference Malinovich et al. (U.S. 6,169,319). The Interview Summary Record states, in relevant part, "Applicant states that the gap between the silicon substrate and the at least one transparent packaging layer, as recited in all of the claims, is not disclosed by Malinovich et al. The Examiner agrees and will further reconsider the rejection, upon receipt of the request for reconsideration from applicant."

Claims 1-4, 6-13, 16-19, 31-32, 37-40 and 55 stand rejected under 35 USC 103(a) as being unpatentable over Malinovich et al. in view of Spaeth et al. Claims 14, 30 and 35 stand rejected under 35 USC 103(a) as being unpatentable over Malinovich et al. and Spaeth et al. in view of Eda et al.

Malinovich et al. discloses a method for producing a CMOS image sensor fabricated on a semiconductor substrate. Spaeth et al. discloses an optoelectronic transducer including a base plate, a radiation-emitting or transmitting semiconductor component disposed on the base plate, an optical lens system and a spacer. Eda et al discloses electronic components formed by directly bonding an insulating layer to a substrate.

In rejecting the claims, the Examiner wrote, "Malinovich et al. disclose(s) (specifically see Figs. 4A-4I) a chip scale package silicon substrate based device comprising: a silicon substrate (300) having formed thereon an optoelectronic structure (100), a chip scale package comprising at least one transparent packaging layer made of glass (410/440) sealed over the optoelectronic structure by an adhesive (e.g., epoxy) layer (420/430) and defining therewith at least one gap between the silicon substrate (300) and the at least one transparent chip scale package layer (410/440), ...". The Applicant respectfully disagrees. While Malinovich et al discloses a chip scale package silicon substrate based device comprising: a silicon substrate (300) having formed thereon an optoelectronic structure (100) and a chip scale package comprising at least one transparent packaging layer made of glass (410/440) sealed over the optoelectronic structure by an adhesive layer (420/430), applicant respectfully submits that the device of Malinovich et al does not disclose a device "defining therewith at least one gap between the silicon substrate (300) and the at least one transparent chip scale package layer (410/440)". A review of Figs. 4A-4I and the description of the method embodied therein (column 6, lines 27 – column 8, line 63) clearly shows that the silicon substrate (300) including the optoelectronic structures (100) is surrounded by adhesive layers 420 and 430 and packaging layers 410 and 440. This specific structure is directly disclosed by Malinovich et al in column 8, lines 5-8:

> Accordingly, each die 300-1 through 300-4 is completely surrounded by epoxy layers 420 and 430, and is sandwiched between protective substrate 410 and transparent substrate 440.

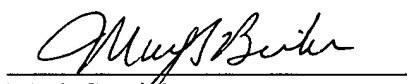
Additionally, neither Spaeth et al. nor Eda et al disclose a chip scale packaged silicon substrate defining therewith at least one gap between the silicon substrate and the at least one transparent chip scale package layer.

With reference to the above discussion, independent claims 1, 10, 37 and 38 are deemed patentable over the prior art of record and favorable reconsideration is respectfully requested. Claims 2-4, 6-9, 30-31, 35 and 55 depend directly or ultimately from claim 1 and recite additional patentable subject matter and therefore are deemed patentable. Claims 11-14, 16-19 and 32 depend directly or ultimately from claim 10 and recite additional patentable subject matter and therefore are deemed patentable. Claims 39-40 depend directly or ultimately from claim 38 and recite additional patentable subject matter and therefore are deemed patentable. As noted hereinabove, Examiner has stated that claims 60-69, 73-74, 76 and 81 are allowable.

Applicant reserves the right to pursue the claims as filed in the context of a continuation application.

In view of the foregoing, all of the claims are deemed to be allowable. Favorable reconsideration and allowance of the application is respectfully requested.

Respectfully submitted,



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